YM2608
OPNA
Application Manual

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Yamaha Motor Co., Ltd.

Outline

YAMAHA sound source LSI OPNA is a compound type sound source system that enhances the function in addition while having interchangeability named OPN(YM2203). The digital rhythm sound source with a high sampling function and reality demanded from the new generation sound source in addition to six FM sound sound pronunciation simultaneously was built into. In addition, it risked it for two channel output.

FM sound source, SSG sound source, ADPCM sound source, and the system configuration by 4 sound source part of the rhythm sound source flexibly correspond to all the sound concepts.

Feature

- FM Sound Source — Four operators six-sound pronunciation simultaneously.
  With built-in sine wave LFO function
  YM2203 and software compatibility full.
- SSG Sound Source — YM2203 and software compatibility full.
  (After mixing, the output outputs 3ch.)
- ADPCM Sound Source — ADPCM voice analysis and synthetic function.
  Accessible of memory that external memory and CPU manage.
  Sampling rate 16KHz max.
- Rhythm Sound Source — Six digital rhythm tones. (pronunciation control by event method)
- DAC output — Exclusive use DAC YM3016. 2ch output.
- Master clock — 8MHz
- Nch-Si gate MOS LSI
- 5V single power supply
- 64pin plastic SDIP

Chapter 1 Composition and Function

1-1: Prime function

The basic function of OPNA can be divided roughly into four sound source part of FM sound source, SSG sound source, and ADPCM sound source and the rhythm sound source.

1) FM sound source part

The basic function of the FM sound source part is the same as OPN(YM2203).
(It is a function that the part is enhanced.)

Pronunciation mode	Four operator FM method and six sound pronunciation simultaneously.
Algorithm	Eight kinds.
Parameter	The register address and refer to the FM sound source part.
LFO function	Sine wave LFO. Pitch (PM) and, it modulates amplitude (AM). The LFO frequency is changeable. AM on/off is possible of PMS, the AMS control, and each operator.
Compound sine wave synthesis	One sound is possible in six sounds.
Timer function	Two kinds of timers of A and B.
Output control	On/off of L and R.

2) SSG sound source part

The SSG sound source part is the same as OPN excluding the output method.

Pronunciation form	Three rectangular liquid sounds + white noise.
Function of each data	Refer to the register address.
Output	It outputs it from one terminal by internal mixing.
I/O port	Eight bit general purpose I/O port x2

3) Rhythm sound source part

The rhythm sound source part is a digital rhythm by ADPCM voice synthesis method to build rhythm ROM into.

Pronunciation tone	6 sounds (bass drum, snare, rim shot, Tamm, cymbals, and high hat cymbals)
Pronunciation control	Event method (It is possible to dump it)
Level control	Each tone independence can control. The total level can control.
Output control	On/off of L and R.

4) ADPCM sound source part

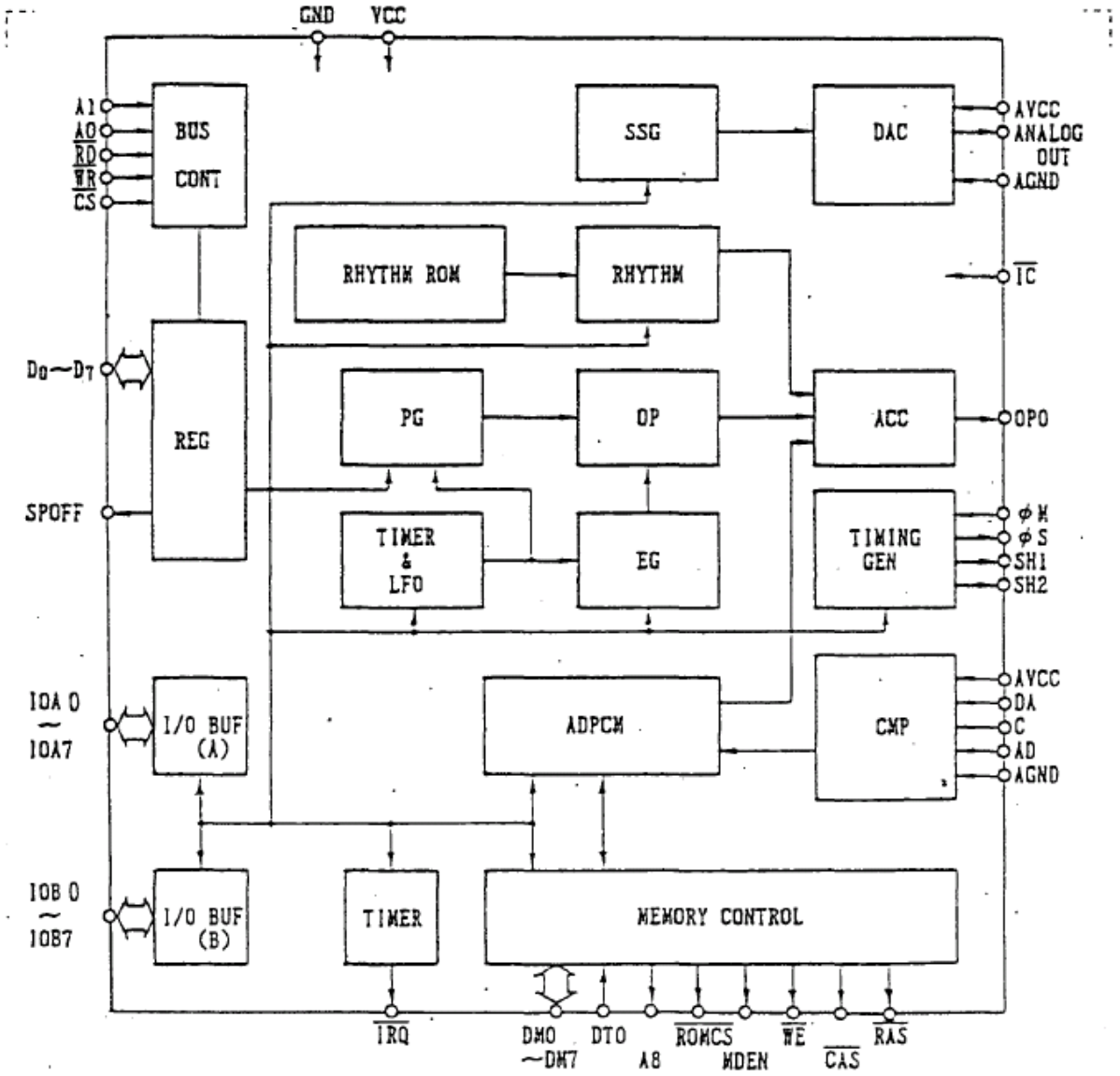
Speech analysis, synthesis, and external memory control of ADPCM sound source part. It is composed of the AD/DA conversion function.

Sampling rate	2kHz-16kHz
AD/DA conversion	8bit
ADPCM analysis	4bit
Linear interpolation rate	55.5kHz
Data memory	Memory that external RAM·ROM or CPU manages.
External memory capacity	256kbytes (max) DRAM access x1bit, x8bit it is possible to select
Output control	On/off of L and R.
No sound discrimination	The state under the analysis of a no sound can be identified.

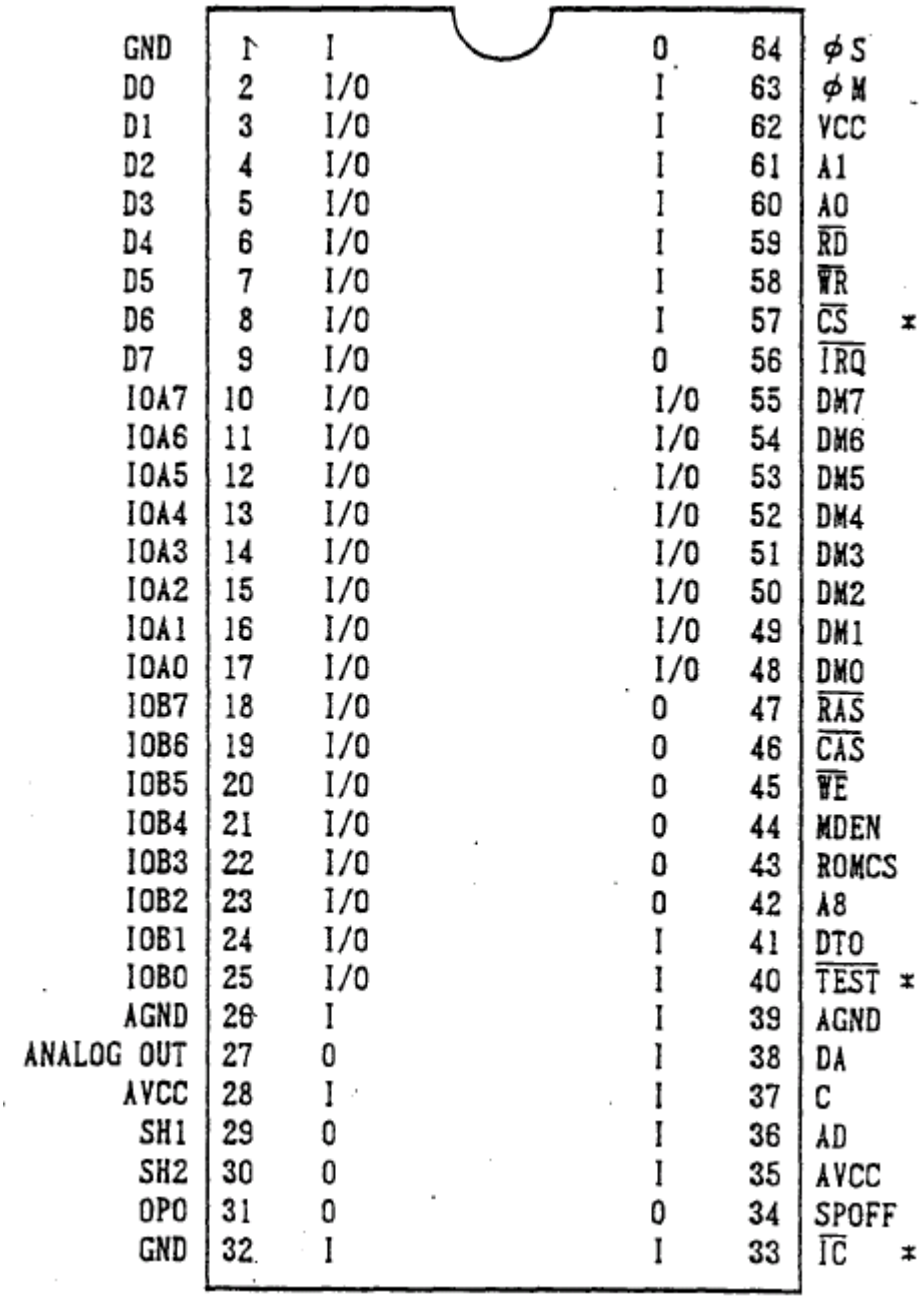
5) DAC

Exclusive use DAC YM3016 is used.

1-2: Block diagram



1-3: Terminal arrangement chart



GND	1	I	O	64	φS
D0	2	I/O	I	63	φM
D1	3	I/O	I	62	VCC
D2	4	I/O	I	61	A1
D3	5	I/O	I	60	A0
D4	6	I/O	I	59	$\overline{RD}$
D5	7	I/O	I	58	$\overline{WR}$
D6	8	I/O	I	57	$\overline{CS}$ *
D7	9	I/O	O	56	$\overline{IRQ}$
IOA7	10	I/O	I/O	55	DM7
IOA6	11	I/O	I/O	54	DM6
IOA5	12	I/O	I/O	53	DM5
IOA4	13	I/O	I/O	52	DM4
IOA3	14	I/O	I/O	51	DM3
IOA2	15	I/O	I/O	50	DM2
IOA1	16	I/O	I/O	49	DM1
IOA0	17	I/O	I/O	48	DM0
IOB7	18	I/O	O	47	$\overline{RAS}$
IOB6	19	I/O	O	46	$\overline{CAS}$
IOB5	20	I/O	O	45	$\overline{WE}$
IOB4	21	I/O	O	44	MDEN
IOB3	22	I/O	O	43	ROMCS
IOB2	23	I/O	O	42	A8
IOB1	24	I/O	I	41	DTO
IOB0	25	I/O	I	40	$\overline{TEST}$ *
AGND	26	I	I	39	AGND
ANALOG OUT	27	O	I	38	DA
AVCC	28	I	I	37	C
SH1	29	O	I	36	AD
SH2	30	O	I	35	AVCC
OPO	31	O	O	34	SPOFF
GND	32	I	I	33	$\overline{IC}$ *

Note: This figure is TOP VIEW.
* It is a pull-up in Vcc. the terminal of the sign

1-4: Terminal function

- ϕM — Master clock (standard 8MHz) of OPNA is input.
- ϕS,SH1,SH2 — It is clock (ϕS) for DAC and signal (SH1, SH2) of the cycle.
- OPO — It is a serial data of FM, ADPCM, and rhythm each sound source part output.
- D0-D7 — It is passing of interactive data of 8bit. CPU and data are exchanged.
- !CS,!RD,!WR,A1,A0 — Data passing (D0-D7) is controlled.
- !IRQ — The interrupt signal is output. It is an open drain output.
- ANALOG OUT — It is an analog output terminal in the SSG sound source part. It is source for an output.
- 10A0-10A7, 10B0-10B7 — It is 8bit general purpose I/O port of two affiliates. It is a pull-up in Vcc.
- DM0-DM7 — Each signal of address (A0-A7), data input (D10-D17), and data output (D01-D07) of an external memory is done to each terminal of corresponding DM0-DM7 in the multiplex.
- A8,DT0 — A8 connects DT0 with data output (D00) in address (A8) of an external memory.
- !RAS,!CAS,!WE — It is a control signal of an external memory.
  When an external memory is DRAM, it is connected with the corresponding each terminal.
  It uses it for latch signal (!RAS·!CAS) of the address for ROM. !RAS : to RAS address. !CAS corresponds to the CAS address.
- MDEN,!ROMCS — It is a timing signal that takes the data of an external memory.
  When MDEN is “1”, DRAM data is put on DM1-DM7 and DT0.
  When !ROMCS is “0”, ROM data is put on DM1-DM7 and DT0.
- AD,C,DA — It is a terminal for the AD conversion.
  AD is an analog input terminal, and the input voltage of convertible AD is a range of Vce/2 ± Vce/4(v).
  The terminal DA is connected with the DAC output with the terminal that inputs a standard voltage when AD is converted.
- SPOFF — It is necessary to separate the amplifier and the speaker to use DA Comparta as a reference voltage generator when AD is converted. This terminal is used as a control terminal for that.
- !IC — The operation of OPNA is initialized.
- !TEST — It is a terminal for the test of LSI.
- GND,AGND — It is a ground terminal.
- Vcc,AVcc — It is a power supply terminal of +5V.

1-5: Data bus control

The data bus control of read/write etc. of addressing and data is done with !CS·!WR·!RD·A1·A0. Figure 1-* and Table 1-1 show the allocation of the register address at this time and the control mode of the register.

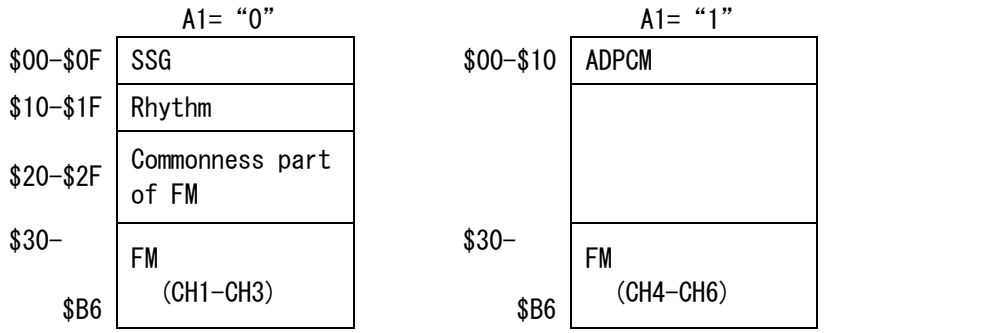


Figure 1-*

Table 1-1: Content of data passing control

!CS	!RD	!WR	A1	A0	Range of address	Content
0	1	0	0	0	00-2F	Addressing of SSG, commonness part of FM, and rhythm
					30-B6	Addressing of FM channel 1-3
0	1	0	0	1	00-2F	Data write of SSG, commonness part of FM, and rhythm
					30-B6	Data write of FM channel 1-3
0	1	0	1	0	00-10	Addressing related to ADPCM
					30-B6	Addressing of FM channel 4-6
0	1	0	1	1	00-10	Data write related to ADPCM
					30-B6	Data write of FM channel 4-6
0	0	1	0	0	XX	Data read of status 0
0	0	1	0	1	00-0F	Read of data of SSG register
					FF	Device identification code read
0	0	1	1	0	XX	Data read of status 1
0	0	1	1	1	08,0F	Read of ADPCM and PCM data
1	X	X	X	X	XX	Inactive mode

(a) READ/WRITE DATA (part SSG)

Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
00	Fine Tune								Channel-A Tone Period
01					Coarse Tune				
02	Fine Tune								Channel-B Tone Period
03					Coarse Tune				
04	Fine Tune								Channel-C Tone Period
05					Coarse Tune				
06				Period Control					Noise Period
07	IN/OUT IOB	IN/OUT IOA	/Noise			/Tone			/ENABLE
08				M	Level				Channel-A Amplitude
09				M	Level				Channel-B Amplitide
0A				M	Level				Channel-C Amplitude
0B	Fine Tune								Envelop Period
0C	Coarse Tune								
0D					CON	ATT	ALT	HLD	Envelop Shape Cycle
0E	I/O PortA								I/O Port Data
0F	I/O PortB								

(b) WRITE DATA (part RHYTHM)

Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
10	DM		RKON						Dump/rhythm KON
11			RTL						Rhythm Total Level
12	TEST								LSI TEST DATA
18 – 1D	L	R		IL					Output Select/Instrument Level

(c) WRITE DATA (FM part)

Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
21	TEST								LSI TEST DATA
22					LFO				LFO FREQ CONTROL
24	TIMER-A								TIMER-A upper 8 Bits
25							TIMER-A		TIMER-A lower 2 Bits
26	TIMER-B								TIMER-B DATA
27	MODE		RESET B	RESET A	ENABLE B	ENABLE A	LOAD B	LOAD A	TIMER-A/B Control and 3 CH Mode
28	SLOT					CH			Key-ON/OFF, CH is specified with D0,D1,D2
29	SCH			IRQ ENABLE					IRQ Enable, SCH
2D									It is Set as for prescaler.
2E									1/3, 1/6 Selection of dividing frequency
2F									The machine of dividing frequency is set to 1/2.
30 - 3E		DT			MULTI				Detune/Multiple (33, 37, 3B There is no Address)
40 - 4E		TL							Total Level (43, 47, 4B There is no Address)
50 - 5E	KS			AR					Key Scale/Attack Rate (53, 57, 5B There is no Address)
60 - 6E	AMON			DR					Decay Rate/AMON (63, 67, 6B There is no Address)
70 - 7E				SR					Sustain Rate (73, 77, 7B There is no Address)
80 - 8E	SL				RR				Sustain Level/Release Rate (83, 87, 8B There is no Address)
90 - 9E					SSG-EG				SSG-Type Envelope Control (93, 97, 9B There is no Address)
A0 A1 A2	F-Num 1								F-Numbers/BLOCK
A4 A5 A6			BLOCK			F-Num 2			
A8 A9 AA	3 CH * F-Num 1								3 CH-3 slot F-Numbers/BLOCK
AC AD AE			3 CH * BLOCK			3 CH * F-Num 2			
B0 B1 B2			FB			CONNECT			Self-Feedback/Connection
B4 B5 B6	L	R	AMS			PMS			PMS/AMS/LR

(d) WRITE DATA (ADPCM part)

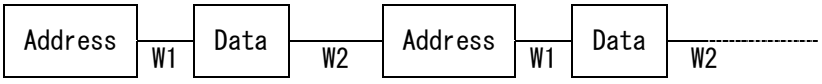
Address	D7 D6 D5 D4 D3 D2 D1 D0
00	CONTROL 1
01	CONTROL 2
02	START ADR (L)
03	START ADR (H)
04	STOP ADR (L)
05	STOP ADR (H)
06	PRESCAL (L)
07	PRESCAL (H)
08	ADPCM-DATA
09	DELTA-N (L)
0A	DELTA-N (H)
0B	EG CTRL
0C	LIMIT ADR (L)
0D	LIMIT ADR (H)
0E	DAC DATA
0F	(PCM DATA)
10	FLAG CONTROL

(e) READ DATA

Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
XX	FLAG								Status 0 (When A1 = “0”) Status 1 (When A1 = “1”)
FF	ID No.								Status 2

1) Addressing mode
Data on the data bus specifies the address of the register when the data bus control is this mode. The specified address is maintained until addressing is done next. Therefore, addressing improves only by the first one time, and is unnecessary afterwards when the data of the same address is continuously accessed.

2) Data write mode
The bus control signal is made <data write mode> after addressing, and data on the data bus is written in the register.



W1: Waiting time after write of address

W2: Waiting time after write of data

In addressing and the data write mode, it is necessary to set each sound source part's prescribed waiting time by moving after writing ends to the following mode. This is because the method of data processing is different in LSI in each sound source part. Please set waiting time to set data in the register correctly. The waiting time when the register of each sound source part is written is indicated in Table 1-* and 1-*.

3) Status read mode
When the bus control signal is made <status read mode>, status information generated in the status register is output on the data bus.

4) Data read mode
The data of the register to be able to read the SSG sound source part and ADPCM sound source part is output on the data bus at <data read mode> time.

5) Inactive mode
When CS is "1", data passing D0-D7 becomes high impedance.

<<Waiting time at writing mode>>

Table *.*: After the write of the address

Sound source part	Address	Waiting cycle
FM	$21-$B6	17
SSG	$00-$0F	0
Rhythm	$10-$1D	17
ADPCM	$00-$10	0

Table *.*: After the write of data

Sound source part	Address	Waiting cycle
FM	$21-$9E	83
	$A0-$B6	47
SSG	$00-$0F	0
Rhythm	$10	576
	$11-$1D	83
ADPCM	$00-$10	0

*Cycle number is cycle of master clock ϕM numbers.

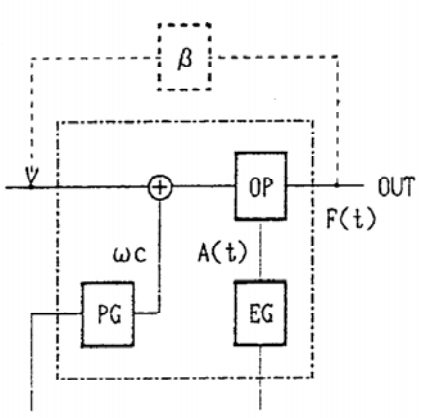
Chapter 2 FM sound source part

The FM sound source part is composed by the register that arranges each parameter to control the LFO block and these that give a periodic change to the operator block and the sound pronounced by four operator FM method by six sounds (color) simultaneously.

2-1: About the FM method
To understand the function of each block in the FM sound source part, it touches a little in the beginning about the FM method. This paragraph doesn't exist needing when the FM sound source is understood enough.
Please start from [2-2 register composition]

2-1-1: Operator
The unit that is called FM operator (cell) that can be shown in the block of Figure 2-1 is prepared in the FM sound source part. The function of this unit can express it like the expression.

$$F(t)=A(t)\sin\omega ct \qquad \text{.....①}$$



OP(operator)
: sin wave generation circuit.
PG(phase generator)
: Frequency (phase) information generation circuit. Data reading speed (ωt) is given to the operator.
EG(envelope generator)
: Operator's output level (A(t)) is controlled.

Figure 2-1: FM operator cell

① The expression shows that FM operator (cell) is a sine wave oscillator of a frequency and a changeable amplitude (envelope). However, it is not so interesting because only the sine wave is output with this as the tone. Then, the tone of a complex overtone composition was made to be able to do the frequency modulation by the sine wave by connecting two or more operators, and to be made. This is FM method.

Two operators are shown and the output when the series is connected is shown in the expression ②.

$$F(t)=A(t)\sin(\omega ct+I(t)\sin\omega mt) \qquad \text{.....②}$$

A(t): Amplitude
I(t): Modulation level
ωc: Frequency of carrier (modulated operator)(phase information)
ωm: Frequency of modulator (modulation operator)(phase information)

In a word, the tone making of the FM sound source can be called work to generate A(t), I(t), ωc, and ωm by controlling PG and EG of the carrier and modulator by each parameter.

Figure 2-2 is a block chart of two operators FM that is the basic configuration of FM method.

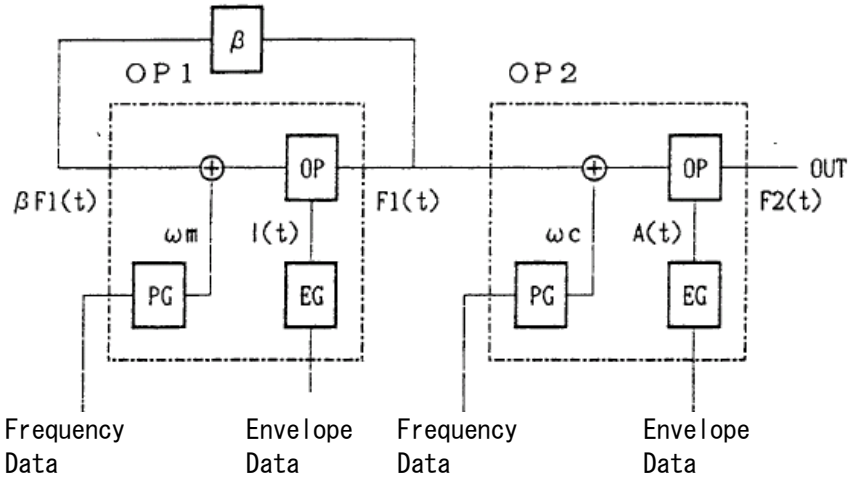


Figure 2-2: Two operator FM

In Figure 2-2, β is a return rate of the self feedback. The self feedback is a method to feed back the output of modulator as a modulation input. The output of OP1 is shown in the expression ③.

$$F1(t)=I(t)\sin(\omega mt+\beta F1(t)) \quad \text{.....③}$$

Because feedback FM is equivalent to the connection of the operator to the series, and the overtone element becomes the harmonic component of the next integer as a result, it is suitable for the tone making a saw blade shape of waves (saw tooth wave) seen in the stringed instrument etc.

FM method can be expressed above by the expression of ①②③. And, a wider sound making is enabled by these combinations. This connection status is called an algorithm (connection). The OPNA connects four operators a sound (1CH). Four operator FM method is adopted, and it will select it from eight kinds of algorithms.

2-1-2: Parameters

When a current thing is brought together, it will only have to set the sound creation of the FM sound source as follows.

- Selection of algorithm
- PG (phase generator) parameter is set, and frequency information is given to the operator.
- EG (envelope generator) parameter is set, and envelope information is given to the operator.
- Setting of β in feedback FM.

The parameter is set by writing data in each register of the FM sound source part.

The parameter that controls each block of operators is as follows.

- Parameter concerning algorithm :Algorithm (Connection), Self-Feedback
- PG parameter :Multiple, Detune, F-numbers, Block
- EG parameter :TotalLevel,
  Attack Rate, Decay Rate, Sustain Rate,
  Sustain Level, Release Rate, SSG-Type EG,
  Key Scale
- LFO parameter :FREQ.CONTROL(LFO SPEED), AMS, PMS, AMON

2-1-3: Channel and slot

OPNA can pronounce 6 sounds (6 channels) at the same time. And, 24 operators in total will be multiplying because they need it by four operators a sound. However, this is a figure for convenience' sake because the FM sound source is understood conceptual, and has only one unit operator cell in LSI. As actual operation of the FM sound source, the operator cell is operated 24 times by the timesharing processing, and six sound pronunciation simultaneously becomes possible.

The state of the operator on the axis of time is expressed in the serial because it operates it like this as the slot. Thereafter, it treats as sound = channel and operator = slot.

2-2: Register composition

The register of the FM sound source part consists of $21-$B6, and the sound creation and the pronunciation control are done by writing suitable data in the register. Moreover, it is classified as follows according to the function.

- $21-$2F: Function that works together compared with all pronunciation channels.
- $30-$9E: Each operator's (slot) tone parameter.
- $A0-$B6: Set parameter and frequency information on each channel.

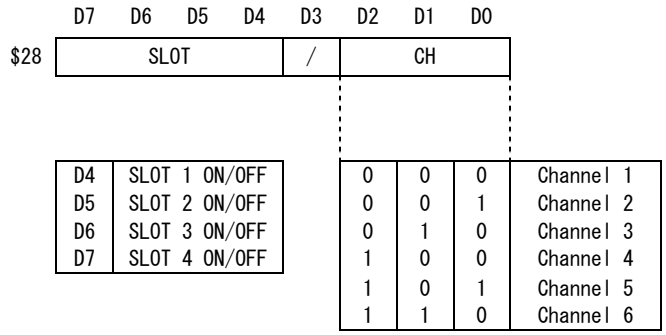
2-2-1: Common register: $21-$2F

- Test: $21
  It is a register for the OPNA test. It doesn't use it in the user application.

- LFO: $22 [Refer to "LFO" page 33]
  It is a register that sets the oscillation frequency of LFO. LFO by the sine wave was enabled on hardware by the function that had been added to OPN(YM2203).

- Timer: $24-27 [Refer to "Timer" page 35]
  They are two kind of timers and registers for the timer controller. The load of CPU is reduced by using it for the pronunciation control etc. of OPNA.

- Key on/off: $28
  The Key assign of each channel is done by on/off of the channel specification and the slot. However, when D7(SCH) of $29 is "0", Channel 4-6 is not good at assign.



□ SCH, IRQ ENABLE: $29

	D7	D6	D5	D4	D3	D2	D1	D0
$29	SCH	/	/	EN ZERO	EN BRDY	EN EOS	EN TB	EN TA

- SCH :It is bit that sets the number of OPNA of pronunciation channels.
  At "0", it is 3 sound (CH1-CH3) pronunciation. <<OPN mode>>
  At "1", it is 6 sound pronunciation simultaneously. <<OPNA mode>>

  A set value is "0" in the early after it initial clears. Please make this bit "1" first to use it by six sound pronunciation simultaneously.
- IRQ ENABLE :The interrupt signal is controlled.
  When each bit of D4-D0 is "1", the terminal !IRQ is made Low level synchronizing with the generation of corresponding status flag.
  The default of D4-D0 is "1".

□ Prescaler function: $2D-$2F

The value of dividing frequency in which FM and the internal operation clock in the SSG sound source part are decided is set. Only these registers write the address data and prescaler is set. The default is FM sound source 1/6, and SSG sound source 1/4.

Table 2-1: Setting of internal clock by prescaler

Addressing	Value n between amounts		The maximum value of master clock :φM max
	FM sound source	SSG sound source	
$2D	1/6	1/4	8MHz
$2D, $2E	1/3	1/2	4MHz
$2F	1/2	1/1	2.67MHz

Internal clock: φINT=φM/n

The prescaler function is an effective function only to FM and the SSG sound source part. Therefore, please use it by the default when you access all sound source parts OPNA. The rhythm and ADPCM sound source part, it provides for the specification of the sampling rate etc. by the value when φM is 8MHz.

2-2-2: Parameters and channel registers: $30-$B6

It is a register that arranges the set data of each operator's (slot) tone parameter and each channel. Table 2-2 shows the register address corresponding to each parameter. The channel is specified by bank changing by bus control signal A1.

→P7　[Refer to 1-5 data to the passing control]

Table 2-2: Relation between register address and channel slot

Slot / Parameter	CH1/CH4				CH2/CH5				CH3/CH6			
	S1	S3	S2	S4	S1	S3	S2	S4	S1	S3	S2	S4
DT/MULTI	30	34	38	3C	31	35	39	3D	32	36	3A	3E
TL	40	44	48	4C	41	45	49	4D	42	46	4A	4E
KS/AR	50	54	58	5C	51	55	59	5D	52	56	5A	5E
AM/DR	60	64	68	6C	61	65	69	6D	62	66	6A	6E
SR	70	74	78	7C	71	75	79	7D	72	76	7A	7E
SL/RR	80	84	88	8C	81	85	89	8D	82	86	8A	8E
SSG-EG	90	94	98	9C	91	95	99	9D	92	96	9A	9E
F-Num1	A0				A1				A2			
Block/F-Num2	A4				A5				A6			
*F-Num1 *1									A9	A8	AA	A2
*Block/F-Num2 *1									AD	AC	AE	A6
FB/Algorithm	B0				B1				B2			
L/R, AMS/PMS	B4				B5				B6			

*1: $A8-$AA and $AC-$AE are registers that set frequency information when channel 3 is made the effect sound mode or CSM voice synthesis mode. Therefore, it doesn't use it in a usual pronunciation mode. Please refer to the ** page for the mode setting of channel 3.

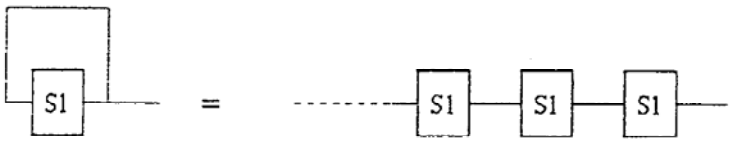
2-3: Algorithm

2-3-1: Algorithm
Operator's combination (connection status) is called the algorithm or a connection. In four operator FM sound source like OPNA, eight kinds of algorithms can be selected. Each slot works by the algorithm as a modulator and a carrier. However, the fourth slot is set to the carrier without fail regardless of the algorithm.

The selection of the algorithm becomes the most important element in the sound creation of the FM sound source. The general procedure of the sound creation is started from the selection of an algorithm that is first of all most suitable for a target tone. Afterwards, the parameter of each slot is set, and the tone will be made. Figure 2-3 shows the form of the algorithm and the feature of each algorithm.

2-3-2: Feedback
In the first slot of each channel, the self feedback function is provided. The self feedback is a function that feeds back own output as a modulation signal by the operator, and self-modulates. Return rate β shows the modulation level, and can set 8 steps of 0-7.

Feedback is equivalent to a serial connection to an operator with the same set of parameters. It becomes it. This effect is suitable for the tone of the vicinity of the spectrum of a high note wave seen in the overtone composition of the next integer to which the high note wave element is thoroughly distributed, that is, in the saw-tooth wave and the strings system. It is more possible in the generation of the noise etc. by deepening the modulation level.



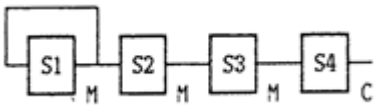
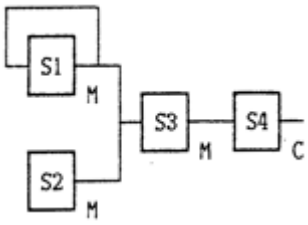
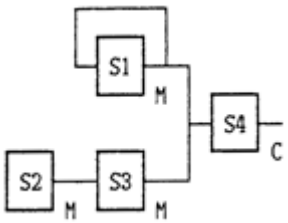
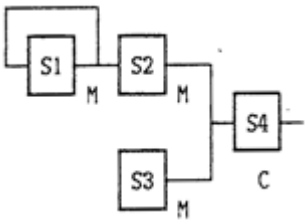
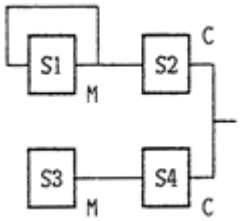
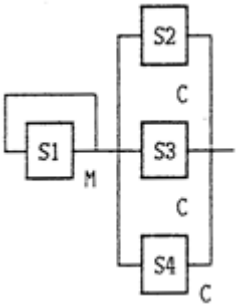
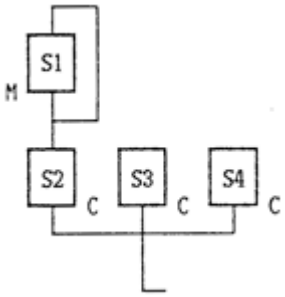
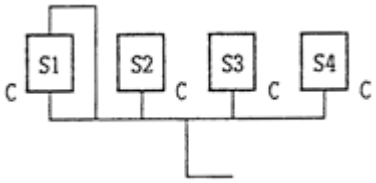
□ FB/Algorithm: $B0-B2
The modulation level of self feedback and the algorithm are set.

	D7	D6	D5	D4	D3	D2	D1	D0
$B0-$B2	/	/	Feedback			Algorithm		

Times of the feedback modulation are read in Table 2-3.

Table 2-3: Feedback modulation level

Feedback	0	1	2	3	4	5	6	7
Modulation level	OFF	$\pi/16$	$\pi/8$	$\pi/4$	$\pi/2$	π	2π	4π

0	Four serial connection mode 	1	Three double modulation serial connection mode 
2	Double modulation mode ① 	3	Double modulation mode ② 
4	Two serial connection and two parallel modes 	5	Common modulation 3 parallel mode 
6	Two serial connection + two sine mode 	7	Four parallel sine synthesis mode 

M:Modulator
C:Carrier

Figure 2-3: Algorithm

1) **Four serial connection mode**
Four slots are connected in series, and it multiple modulates. The multiple modulation method obtains a very complex overtone composition in the final carrier output as a result of the repetition of a continuous modulation and is. The tone that is basic by S4 and S3 is made, the overtone element is adjusted in S2 and S1, and a slight tone is seasoned.

2) **Three double modulation serial connection mode**
S3 is modulated because of a synthetic output of S2 and S1. 1) A basic tone is made from similar and S4 and S3, and a more detailed sound making is done in stripes a by setting the parameter of S2 and S1.

3) **Double modulation mode ①**
S4 is modulated by modulator of two affiliates. The tone that is basic makes from S1 and S4, and adds the addition sound in which a natural feeling is given to the tone with S2 and S3.

4) **Double modulation mode ②**
3) Because it is not put to feed back to S3 self, it is suitable for the sound of the fluty woodwind though does to look like well. The noise element is made in S2 and S1.

Because the carrier is 1 piece in 1)-4), it is suitable for the sound making of a single tone. It is suitable for tones of the solo musical instruments with a complex overtone element.

5) **Two serial connection and two parallel modes**
It is an algorithm of two operator two affiliate composition. Because the sound creation is an easy thing comparatively and can make two kinds of tones, this mode can be used for a wide sound making though is a little unsuitable for the tone with a lot of overtone elements.

6) **Common modulation 3 parallel mode**
Common modulator S1 modulates carrier S2, S3, and three S4.

7) **Two serial connections + two sine mode**
A synthetic output of one two operator FM and two sine waves is obtained.

8) **Four parallel sine wave synthesis mode**
The output that synthesizes four sine waves is obtained. However, S1 can make the sound distorted by putting feedback.

In the algorithm which the plural becomes the carrier, the parameter concerning frequency information becomes the conclusive evidence of the sound creation. In the algorithm “7”, the effect of the coupler like the organ sound is achieved by changing the multiple of each carrier. In addition, undulation is achieved in the sound by slightly moving the pitch by setting detune and causing, so-called the effect of the chorus (detune), is achieved.

2-4: PG(phase generator)
The output frequency of the operator is decided depending on frequency (phase) information where PG (phase generator) is generated. In a word, the pronunciation by an arbitrary frequency is possible by the increase and decrease of the phase data. The phase value, that is, frequency information is obtained because of the setting of each parameter of F-Number/Block, Multiple, and Detune.

2-4-1: F-Number/Block
The music scale of the tone can be shown by the interval and the octave of one octave. Then, if the interval in one octave is made from F-Number, and octave information is set with Block, the music scale of eight octaves can be easily made.

The F-Number setting value in one octave can be calculated by using the next expression if it is decided that the master clock is a frequency of the interval.

$$F\text{-Number} = (144 * fnote * 2^{20} / \phi M) / 2^{B-1}$$

fnote: Pronunciation frequency
ϕM: Master clock
B: Block data

(example) F-Number of A4 (440Hz) is obtained at ϕM=8MHz.

$$F\text{-Number(A4)} = (144*440*2^{20} / 8*10^{6}) / 2^{4-1}$$
$$= 1038.1$$

□ F-Number/Block: $A0-$A2/$A4-$A6

It is a register that sets F-Number and the Block data. As for F-Number, subordinate position 8bit/high rank 3bit with 11bit total. Block is composed of 3bit. This data is used as common data to the channel. The four operators are given the same information.

	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
A4-A6 /A0-A2	/	/	Block			F-Num2			F-Num1							

F-Number/Block Please set data according to the following procedures.
①Data write of Block/F-Num2: $A4-$A6 ②Data write of F-Num1: $A0-$A2

[Reference]

A. Example of setting F-Number table

Table 2-4: F-Number table
ϕM = 8MHz, Octave :4 ($C4^{\#}$-C5), A4=440Hz.

Note	Interval [Hz]	F-Number	F11-F9			F8-F5				F4-F1				Key Code		
			D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	N4	N3	Division
C#	277.2	654.0	0	1	0	1	0	0	0	1	1	1	0	0	0	0
D	293.7	692.8	0	1	0	1	0	1	1	0	1	0	0	0	0	0
D#	311.1	734.0	0	1	0	1	1	0	1	1	1	1	0	0	0	0
E	329.6	777.7	0	1	1	0	0	0	0	1	0	0	1	0	0	0
F	349.2	823.9	0	1	1	0	0	1	1	0	1	1	1	0	0	0
F#	370.0	872.9	0	1	1	0	1	1	0	1	0		0	0	0	0
G	392.0	924.8	0	1	1	1	0	0	1	1	1	0	0	0	1	1
G#	415.3	979.8	0	1	1	1	1	0	1	0	0	1	1	0	1	1
A	440.0	1038.1	1	0	0	0	0	0	0	1	1	1	0	1	0	2
A#	466.2	1099.8	1	0	0	0	1	0	0	1	1	0	0	1	0	2
B	493.9	1165.2	1	0	0	1	0	0	0	1	1	0	1	1	1	3
C	523.3	1234.5	1	0	0	1	1	0	1	0	0	1	0	1	1	3

B. Setting of KeyCode
When the F-Number data is decided, detune, and Key-Code to give the key scaling to the envelope rate is set. The key scaling is a function to change the pitch gap by detune and the envelope rate according to the pronunciation interval.

Key-Code is set by the frequency division in one octave based on the F-Number data and combining the Block data.

* Frequency division in one octave(N4,N3)

  N4=F11
  N3=F11・(F10+F9+F8) + !F11・F10・F9・F8

* Key-Code in 32 stages is set from total 5bit of Block data (B3,B2,B1) and above-mentioned N4 and N3 in eight octave whole tone region, and the key is scaled.

2-4-2: Multiple

Multiple is a parameter that sets the magnification to frequency information made from F-Number/Block in addition. The magnification that can be set is Table 2-5.

2-4-3: Detune

Detune is a parameter that gives cycle several gap slight in each slot as for frequency information made from F-Number. Moreover, Detune takes the value corresponding to each frequency information by Key Code obtained from F-Number.

□ Detune/Multiple

	D7	D6	D5	D4	D3	D2	D1	D0
$30-3E	/	Detune			Multiple			

Table 2-5: Magnification by Multiple

Multiple(H)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Magnification	1/2	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Table 2-6: Detune

Detune	0	1	2	3	4	5	6	7
FD	0	1	2	3	0	-1	-2	-3

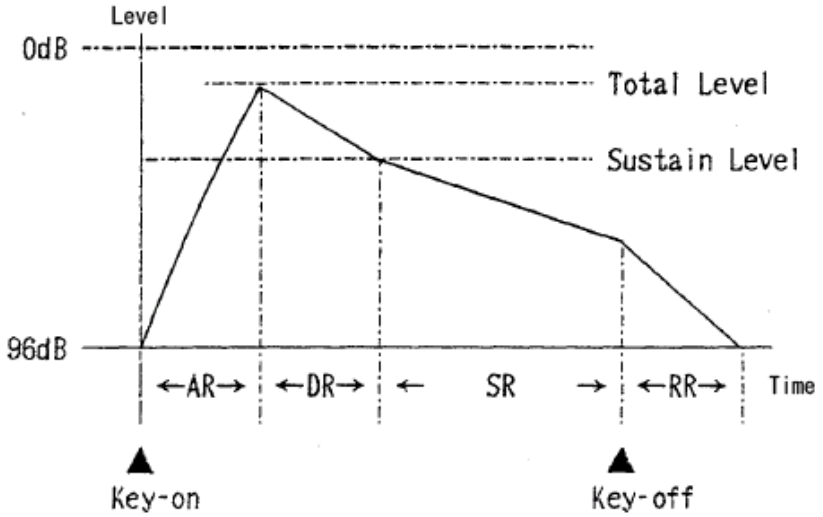
*D6 is a sign bit

BLOCK	NOTE	FD=0	FD=1	FD=2	FD=3	BLOCK	NOTE	FD=0	FD=1	FD=2	FD=3
0	0	0.000	0.000	0.053	0.106	4	0	0.000	0.106	0.264	0.423
0	1	↑	↑	↑	↑	4	1	↑	0.159	0.317	0.423
0	2	↑	↑	↑	↑	4	2	↑	↑	↑	0.476
0	3	↑	↑	↑	↑	4	3	↑	↑	0.370	0.529
1	0	↑	0.053	0.106	↑	5	0	↑	0.212	0.423	0.582
1	1	↑	↑	↑	0.159	5	1	↑	↑	↑	0.635
1	2	↑	↑	↑	↑	5	2	↑	↑	0.476	0.688
1	3	↑	↑	↑	↑	5	3	↑	0.264	0.529	0.741
2	0	↑	↑	↑	0.212	6	0	↑	↑	0.582	0.846
2	1	↑	↑	0.159	↑	6	1	↑	0.317	0.635	0.899
2	2	↑	↑	↑	↑	6	2	↑	↑	0.688	1.005
2	3	↑	↑	↑	0.264	6	3	↑	0.370	0.741	1.058
3	0	↑	0.106	0.212	↑	7	0	↑	0.423	0.846	1.164
3	1	↑	↑	↑	0.317	7	1	↑	↑	↑	↑
3	2	↑	↑	↑	↑	7	2	↑	↑	↑	↑
3	3	0.000	↑	0.264	0.370	7	3	0.000	↑	↑	↑

[Unit: Hz]

2-5: EG(envelope generator)
EG (envelope generator) is a block where a time change in the volume and the tone from standing up of the sound to the disappearance occurs. The envelope generator that generates the envelope is being composed of the output control circuit decided a whole level by EG. Information to start EG can be set to each operator according to the parameter for EG arranged in the register.

2-5-1: Envelope generator
The envelope that forms a time change in the sound is generated. The envelope attacks, and is shown by each rate and sustain level of decay, sustain, and release. Figure 2-4 shows the envelope wave form and each parameter.



* The shape of waves of the envelope changes in exponential when attacking it, and it changes in the straight line at other rates.

Figure 2-4: Shape of waves and each parameter of envelope

□ AR (Attack Rate) :$50-$5E
The attack rate is a speed that reaches the utmost level since the moment when Key-on was done, and AR is a parameter that decides this rate. 32 steps can be set. Standing up of the sound quickens by AR large. Moreover, the attack rate becomes infinity, and the envelope doesn't start at "0".

	D7	D6	D5	D4	D3	D2	D1	D0
$50-5E	KS		/	Attack Rate				

* Refer to page 29 for KS

□ DR (Decay Rate) :$60-$6E

Decay rate is a speed from the utmost level after the attack time passes from which everything reaches sustain level, and DR is a parameter that decides this rate. 32 steps can be set, and it attenuates faster the larger DR is. Moreover, decay rate becomes infinity, and it becomes a continuation sound by the utmost level at “0”.

	D7	D6	D5	D4	D3	D2	D1	D0
$60-6E	AM	/	/	Decay Rate				

*Refer to page 34 for AM

□ SL (Sustain Level) :$80-$8E

Sustain level is the level (amount of attenuation) that changes from decay rate into sustain rate, and SL is a parameter that decides this level. The amount of attenuation grows by can the setting of 16 steps, and SL large. The amount of attenuation becomes 0 when making it to “0”, and the attenuation feeling by decay is not obtained. The weight putting of each bit is Table 2-7.

	D7	D6	D5	D4	D3	D2	D1	D0
$80-8E	Sustain Level				Release Rate			

Table 2-7: Weight putting of SL each bit

	D7	D6	D5	D4
Amount of attenuation(dB)	24	12	6	3

* When D7-D4 is entire “1”, it becomes 93dB.

□ SR (Sustain Rate) :$70-$7E

Sustain rate is a speed that attenuates from sustain level, and SR is a parameter that decides this rate. Attenuation quickens by can the setting of 32 steps, and SR large. Moreover, it continues with sustain level when making it to “0”.

	D7	D6	D5	D4	D3	D2	D1	D0
$70-7E	/	/	/	Sustain Rate				

□ RR (Release Rate) :$80-8E

The release rate is Key off speed of the following attenuation, and RR is a parameter that decides this rate. Attenuation quickens by can the setting of 16 steps, and RR large.

Five parameters are set, and operator's envelope is decided above. However, the envelope of the same rate will be given to the operator regardless of the height of the output frequency of the operator it is possible to hold this, and it be unnatural depending on the tone. Then, the envelope rate has been changed by the key scaling function according to the interval.

- KS (Key-Scale) :$50-$5E
  The key scale is a function to change the rate of the envelope according to the pronunciation interval. In this case, the rate shortens by becoming the high pitched sound degree, and a natural feeling can be given to the tone. Four steps can be set. The key scale doesn't function in "0", and differences grow most at "3" (time).

  The key scaling value of the rate by KS is indicated in Table 2-8.

Table 2-8: Key-Scaling value of Rate

Block / Note	0				1				2				3			
	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
0	0								1							
1	0				1				2				3			
2	0		1		2		3		4		5		6		7	
3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Block / Note	4				5				6				7			
	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
0	2								3							
1	4				5				6				7			
2	8		9		10		11		12		13		14		15	
3	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Each rate of the envelope generator is finally decided by the offset value given by the setting data and the key scaling about the ADSR parameter. This value is as shown in the next expression.

Rate = 2R + Rks　　;Rate = 0 in case of R = 0

- R is a set value of each parameter of ASDR.
  However, RR(Release Rate) (Set value * 2 + 1) is assumed to be R.
- Rks is a key scaling value.

*The maximum of Rate is 63, and everything is assumed to be Rate=63 at the value whose calculation result is bigger than 63.

2-5-2: SSG-type Envelope Control

The envelope generator can be controlled according to the envelope wave form of SSG-type. This uses the envelope wave form of the SSG sound source part, and the change in the envelope not obtained only by the parameter for EG can be applied. The shape of the envelope is shown in (figure below).

Please set the EG parameter as follows when you use this envelope.

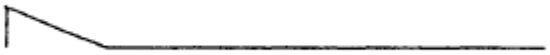
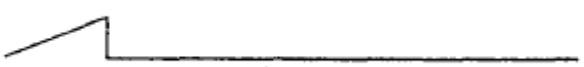
① AR is fixed to “1F”.

② The change in the envelope in the state of Key-on is decided by the level setting by DR, SR, and SL.

③ RR works as well as a usual mode, and the following attenuation time of Key-off is decided.

□ SSG-EG :$90-9E

	D7	D6	D5	D4	D3	D2	D1	D0
$90-9E	/	/	/	/	SSG-EG			

No.	D3	D2	D1	D0	Envelope shape
0	1	0	0	0	
1	1	0	0	1	
2	1	0	1	0	
3	1	0	1	1	
4	1	1	0	0	
5	1	1	0	1	
6	1	1	1	0	
7	1	1	1	1	

2-5-3: Output control circuit
As for the envelope made from the EG parameter, a whole level is set with the output control circuit. As a result, operator's output level is decided, and the resolution that can be set by 96dB is 0.75dB in the dynamic range.

The output level is to be shown by the amount of attenuation as a point noted here. In a word, the amount of attenuation when the maximum value of the output of the operator is assumed to be 0dB will be set.

- TL (Total Level) :$40-$4E
  The output level is set at the total level. The weight putting of each bit shows the amount of attenuation. Therefore, it is "00" and 0dB (utmost level) It becomes amount 96dB of attenuation (minimum level) by "7F".

	D7	D6	D5	D4	D3	D2	D1	D0
$40-4E	/	Total Level						

Table 2-9: Weight putting of TL each bit

	D6	D5	D4	D3	D2	D1	D0
Amount of Attenuation(dB)	48	24	12	6	3	1.5	0.75

2-6: LFO: Low Frequency Oscillator

LFO is a function to modulate the operator because of the output of the low frequency oscillator of building into, and for a periodic change to give to the sound. The LFO shape of waves of OPNA controls the modulation according to five kinds of parameters because of the sine wave.

□ LFO FREQ. :$22

The on/off control of LFO and the speed of LFO (oscillation frequency) are set.

	D7	D6	D5	D4	D3	D2	D1	D0
$22	/	/	/	/	ON	FREQ.CONT		

D3 : LFO on at “1”.
D2-D0 : Setting of LFO speed (oscillation frequency).

FREQ.CONT	0	1	2	3	4	5	6	7
freq(Hz)	3.98	5.56	6.02	6.37	6.88	9.63	48.1	72.2

□ PMS (Phase Modulation Sensitivity) :$B4-$B6

To frequency (phase) information set with F-Number/Block, by adding LFO (Modulate), it to be able to be obtaining of a periodic change in the interval. PMS is a parameter that sets depth and the phase modulation degree of the modulation of each channel.

□ AMS (Amplitude Modulation Sensitivity) :$B4-B6

A periodic change is given at operator's output level. AMS is a parameter that sets depth and the amplitude modulation degree of the modulation of each channel. The effect on the sound at the amplitude modulation caused by LFO is given in operator's role. It becomes a change in the volume, and the tone changes in modulator when the carrier is modulated.

	D7	D6	D5	D4	D3	D2	D1	D0
$B4-$B6	L	R	AMS		/	PMS		

Refer to page 35 for L,R

PMS	0	1	2	3	4	5	6	7
Modulation level (cent)	0	3.4	6.7	10	14	20	40	80

AMS	0	1	2	3
Modulation level (dB)	0	1.4	5.9	11.8

□ AMON: $60-$6E

It is a switch to do on/off of the amplitude modulation to each slot. On at “1”.

	D7	D6	D5	D4	D3	D2	D1	D0
$60-$6E	AMON	/	/	Decay Rate				

When an enough effect is not achieved because of sine wave LFO of building into, software LFO (saw-tooth wave, rectangular wave, triangular wave, and S/H, etc) is necessary. This will only have to give data corresponding to the LFO shape of waves to operator's each parameter by the interrupt processing using the timer of building into.

Figure 2-5 shows the block chart of the LFO function.

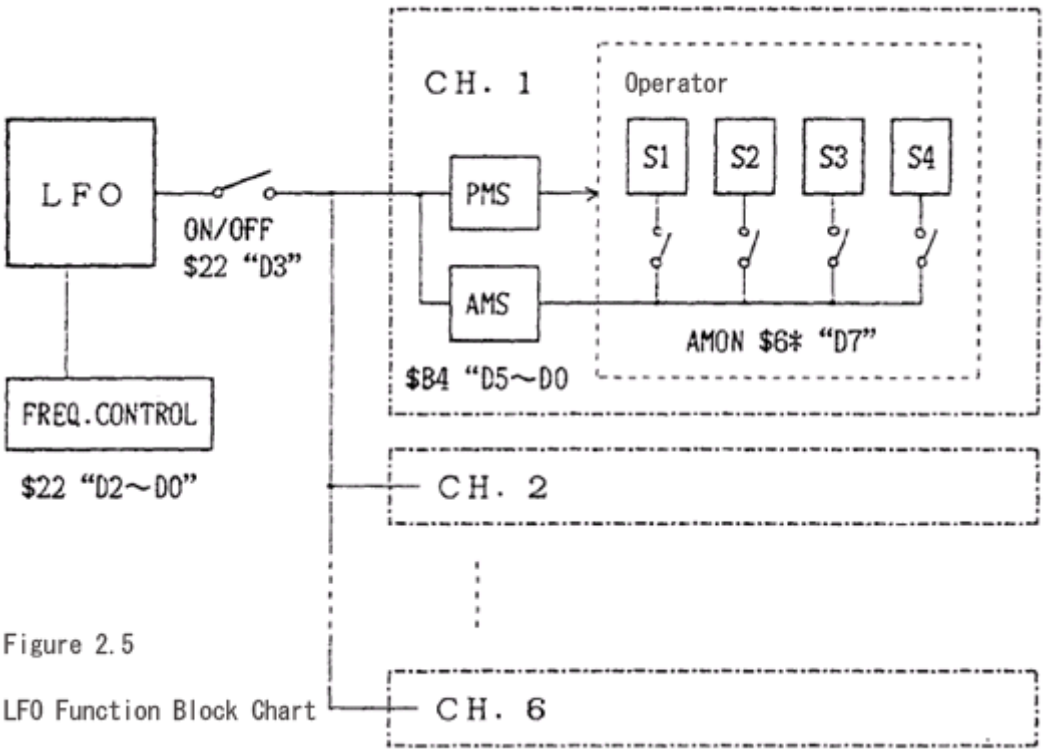


Figure 2.5

LFO Function Block Chart

[Reference]

As for a periodic change in the sound by LFO, the following effects on the tone are achieved.

- Change in interval (pitch): Vibrato
- Change in volume (level): Tremolo
- Change in tone (tone): WOWOW

2-7: Output selection
LCH and the sentence are switches specified for RCH as for the output of the FM sound source part.

- L/R: $B4-B6 “D7, D6”
  It becomes turning on by “1”, and it outputs it to the CH.

2-8: Timer
The timer is composed of the timer controller of two kinds of presettable timers and flags which start, stop, and control the timers. Timer information sets up “1” in timer flags (D1,D0) of status 0 and 1 when the time set to the timer passes, and generates IRQ for CPU.

2-8-1: Timer A
Timer A is a timer counter of resolution 9μs (at φM=8MHz) made from 10bit of $24 and $25. The interval of time that can be set can be calculated by expression ①.

	D7	D6	D5	D4	D3	D2	D1	D0
$24	P9	P8	P7	P6	P5	P4	P3	P2
$25	/	/	/	/	/	/	P1	P0

tA = 72 * (1024 - NA) / φM
NA: 0-1023
φM: Master clock

(example) φM=8MHz time
tA(MAX) = 9216μs
ta(MIN) = 9μs

2-8-2: Timer B
Timer B is a timer counter of resolution 144μs (φM=8MHz) made from 8bit of $26. The interval of time that can be set can be calculated by the expression ②.

	D7	D6	D5	D4	D3	D2	D1	D0
$26	P7	P6	P5	P4	P3	P2	P1	P0

tB = 1152 * (256 - NB) / φM
NB: 0-255
φM: Master clock

2-8-3: Timer controller
Timer A and B are controlled by the timer controller of $27.

	D7	D6	D5	D4	D3	D2	D1	D0
$27	MODE		RESET		ENABLE		LOAD	
			B	A	B	A	B	A

D1,D0: The timer is started, and the stop is controlled.
"1" - It starts
"0" - The timer stops

D3,D2: Timer flags of status 0 and 1 are controlled.
"1" - Stands in the timer flag at the same time as the timer counter's overflowing at "1". Moreover, this timer flag generates interrupt signal (LOW) in the terminal !IRQ.
"0" - Even if the timer counter overflows, the timer flag is not changed.

D5,D4: The timer flag is reset.
"1" - Timer flags of status 0 and 1 are reset. This bit is cleared to "0" at the same time.

2-8-4: Setting of mode of CH3
Channel 3 can set the mode by $27 "D7,D6".

Table 2-1C: CH3 mode

D7	D6	Mode	Function
0	0	Normality	It pronounces normally as well as other CH.
0	1	CSM	It becomes CSM voice synthesis mode, and F-Number can be set each every of the four slots. Key-on/off at the CSM mode is done with timer A.
1 1	0 0	Effect sound	Separate F-Number can be set to each slot as well as CSM.

Chapter 3 SSG sound source part

The tone of the analog signal (SSG sound) is output from the output terminal of OPNA(pin 27; ANALOG OUT). The register of SSG is different from the FM sound source part, and read/write is possible. It explains each register as follows as the function of the SSG sound source part.

3-1: Tone generator control
A rectangular wave of 1:1 compared with the duty can be pronounced by three sounds in the SSG sound source part simultaneously. The tone generator control sets the pronunciation frequency of channel A, B, and C by the data of 12bit in total of rough adjustment 4bit and fine-tuning 8bit. The expression from which the pronunciation frequency is requested is as follows.

ftone = ϕM / (64*TP)

ϕM: Mastering clock frequency
TP: Pronunciation frequency setting value(decimal number of 12bit)

- Fine Tune: $00,$02,$04
- Coarse Tune: $01,$03,$05

	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
$01・$00 $03・$02 $05・$04	/	/	/	/	Coarse Tune				Fine Tune							

*Range of frequency that can be pronounced: TP=4095(MAX)- 1(MIN)

ftone(MIN)= ϕM / 262,080
ftone(MAX)= ϕM / 64

3-2: Noise generator control
In addition, the noise generator by a pseudoand random wave form is built into the SSG sound source part. The noise frequency is set by the noise generator control.

fnoise= ϕM / (64*NP)

ϕM: Mastering clock frequency
NP: Noise frequency setting value(decimal number of 5bit)

- Noise Period: $06

	D7	D6	D5	D4	D3	D2	D1	D0
$06	/	/	/	Noise Period				

3-3: Mixer and I/O control
This register controls I/O mode of on/off of each channel of the tone (tone) and the noise generator and general purpose I/O port of two affiliates.

□ !IN/OUT, !NOISE, !TONE

	D7	D6	D5	D4	D3	D2	D1	D0
$07	IN/OUT		!NOISE			!TONE		
	IOB	IOA	C	B	A	C	B	A

D7,D6: The I/O of the I/O port is controlled.
It becomes an output by input and "1" in "0".
D5-D3: The output channel of the noise is set.
It outputs it by "0".
D2-D0: Channel on/off of the tone generator is set.
It outputs it by "0".

3-4: Level control
The output level of channel A, B, and C is controlled. The output level can select the envelope level mode that applies a time change to the fixed level mode and the volume output by a constant volume.

□ M/Lebel: $08-$0A

	D7	D6	D5	D4	D3	D2	D1	D0
$08-$0A	/	/	/	M	Lebel			

D4: The mode is selected.
At "0", it becomes a fixed output level set with D3-D0.
At "1", the output level changes corresponding to the envelope generator.
D3-D0: The output level is set.
It becomes the maximum level by all "1".
When D4 is "1", this bit is Don't care.

Table 3-1 Weight putting of Level each bit

	D3	D2	D1	D0	
DAC data	L5	L4	L3	L2	L1
Output level	16	8	4	2	1

*When you assume the utmost level to be 31. However, all "0" is level 1.

3-5: Envelope generator control
When the output level of channel A, B, and C is made an envelope level mode, a time change can be given at the output level according to the shape of the envelope. In the following registers, the cycle of the envelope wave form and the repetition is set.

- Fine Tune: $0B
- Coarse Tune: $0C

	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
$0C,$0B	Coarse Tune								Fine Tune							

The setting of data is earned to $0B and $0C, and the repetition frequency of the envelope generator is requested as shown in the next expression.

$$F\,EG = \phi M / (1024*EP)$$

ϕM: Mastering clock frequency.
EP: Cycle given by $0C and $0B set value (decimal number).

As a result, cycle tEG is given by 1/fEG.

- C/ATT/ALT/HLD: $0D
  It is a register that sets the envelope wave form. Eight kinds of envelopes can be selected with 4bit of D3-D0. The wave form of each envelope wave form is equal to FM sound source on page 31 part SSG-EG.

	D7	D6	D5	D4	D3	D2	D1	D0
$0D	/	/	/	/	C	ATT	ALT	HLD

<<About the SSG output>>
After it is converted into the analog voltage with DAC only for the channel, channel A, B, and C output are output from mixing ANALOG OUT (pin 27) terminal in LSI. Therefore, mixing need not be done by the external resistance done by a past SSG type. However, because it is “source for an output”, load resistance (RL) is necessary. The output voltage is 1Vp-p (At RL=470Ω, three sound pronunciation simultaneously, and an output maximum level).

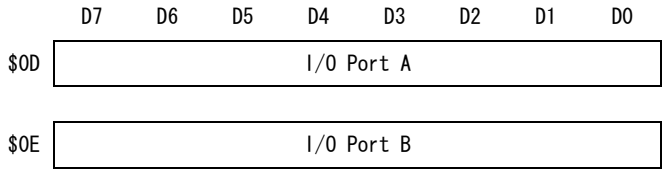
As for building DAC into, the output level is obtained in the logarithm step of 5bit. Then, when the output mode is a fixed output, the level of 16 steps can be set from the maximum to the minimum by setting the data of high rank 4bit. Moreover, at the envelope output, for one envelope cycle in giving the increase and decrease value of the data of 5bit to DAC, The level changes continuously by the specified envelope wave form. The step of the change in this time is 31 steps (0 and 1 falls on same level).

3-6: I/O port

General purpose I/O port of two affiliates is built into the SSG sound source part. This I/O port can be used as an enhancing port for the interface of CPU and an external system.

□ I/O Port A,B: $0E, $0F

It is a register of the storage of the I/O data of the I/O port. When the port is used as an output, data is written from CPU. When using it as an input, data from an external system is set.



<<Attention when I/O port is controlled>>

① The I/O of the I/O port is set with D7 and D6 of $07. Therefore, please specify I/O mode for read/write of $0E and $0F with ahead and $07.

② When the port is specified for the output mode, it keeps outputting the data written in the register from the port until being held, and being updated to the fresh data. However, initial clearness, or when the port is changed to the input mode, it excludes it.

③ When OPNA is !IC (Initial clearness: 192 cycles or more of ϕM), the I/O port becomes an input mode.

④ Please do not add the input voltage to the terminal I/O when the port is an output mode.

Chapter 4 RHYTHM sound source part

The rhythm sound source part is a digital rhythm tone that uses ADPCM voice synthesis. ADPCM rhythm tone can pronounce tones of the rhythm musical instruments that the sound making is difficult with easy software in the FM sound source. Moreover, the rhythm tone can comparatively sample easily because of the attenuation sound by a little memory, and secure the envelope from the generation of the sound to the disappearance naturally.

The tone is composed of six kinds of drums of a basic tone, and can be pronounced by six sounds simultaneously. Because each tone can individually set the level, the accent processing to say nothing of the balance adjustments of each musical instrument can be freely done.

The control register of the rhythm sound source part is composed of $10-$1D. Moreover, when bus control signal A1 is “0”, the data access to this register is possible.
(Refer to seven pages to the bus control)

It explains the function of each register as follows.

□ DM/RKON (Dump/Rhythm Key on): $10
On/off of the rhythm is controlled by the event method. The rhythm sound specified with D5-D0 pronounces when DM is “0”, and it attenuates naturally by the envelope of each rhythm. When DM is “1”, the specified rhythm sound is compulsorily dumped (muffle). The relapse sound or the compulsion dump (mute) under attenuation is done according to the timing of a new event.

	D7	D6	D5	D4	D3	D2	D1	D0
$10	DM	/	RIM	TOM	HH	TOP	SD	BD

D7: Dump at “1”. Key on at “0”.
D5-D0: Each rhythm sound specification.

□ RTL (Rhythm Total Level): $11
It is an integrated volume of the rhythm sound source part. Even -47.25-0dB controls the level by 64 steps. Resolution is 0.75dB.

	D7	D6	D5	D4	D3	D2	D1	D0
$11	/	/	RTL					

	D5	D4	D3	D2	D1	D0
Amount of attenuation(dB)	24	12	6	3	1.5	0.75

D5-D0: At all “0”, -47.5db.
At all “1”, 0db.

□ Test: $12
It is a register for the test of OPNA. An initial value is all “0”.

□ LR/IL (Output Selection/Instrument Level)
The control and the output channel at the level of each rhythm tone are specified.
The level is controlled up to -23.25-0dB by 32 steps. Resolution is 0.75dB.

	D7	D6	D5	D4	D3	D2	D1	D0
$18-$1D	L	R	/	IL				

	D4	D3	D2	D1	D0
Amount of attenuation(dB)	12	6	3	1.5	0.75

D7: At “1”, it outputs it to LCH.
D6: At “1”, it outputs it to RCH.
D4-D0: At all “0”, -23.25db.
At all “1”, 0db.

The register corresponding to the tone is as follows.

$18: BD (bass drum)
$19: SD (snare drum)
$1A: TOP (top cymbals)
$1B: HH (high hat cymbals (X))
$1C: TOM (tam-tam)
$1D: RYM (rim shot)

Chapter 5 ADPCM sound source part

ADPCM sound source part is a speech analysis and is synthesized by using the data compression technology by ADPCM method. The ADPCM(Adaptive Differrential PCM) method is able not to ruin tone quality so much by encoding the difference between the voice data and the forecast data according to the width of the quantization (width of the adjustment quantization) that flexibly changes into the displacement of the shape of waves and to attempt the reduction in volume of information (bit rate) necessary for the reproduction.

It is possible to pronounce simultaneously with the FM, SSG, and rhythm sound source parts by sampling the genuine sound quality of a human voice and the natural world by building ADPCM sound source into.

5-1: Prime function

1) ADPCM voice analysis and synthesis

   4bit ADPCM voice analysis/is synthesized.
   When analyzing it, the sampling rate: 2kHz-16kHz.
   At synthesis: 2kHz-55.5kHz can be set.

   Speech analysis/synthesis is executable between external memory 1 or CPU (However, management memory) of OPNA. In addition, the data transfer can be done from CPU to an external memory from an external memory to CPU through OPNA.

2) External memory control
   The data access when speech analysis/synthesizing it to the external memory that OPNA manages is controlled. RAM/ROM can select both accesses of DRAM in possible external an amount of memory with 256kbyts and x1bit or x8bit and ROM be selected.

3) AD/DA conversion
   It is possible to use it by using exclusive use DAC･YM3016 as AD or DA converter.
   In any case, the sampling rate is done between 2kHz-16kHz.

[Reference] Algorithm of ADPCM

A. Procedure of ADPCM voice analysis

① AD conversion — The voice is converted into the PCM data of 8bit in each sampling rate.

② 8->16 conversion — 256 obtained PCM data is multiplied, and the data of 16bit; It converts it into Xn.

③ Calculation of dn — This Xn is compared with forecast value ^xn, and the difference; dn is obtained.

④ Decision of ADPCM data

It is "0" that dn is positive as for MSB(L4) of ADPCM data. It makes it to "1" negatively.
Absolute value of difference; |dn| Width of quantization; Remainder 3bit(L3,L2,L1) of ADPCM data is decided from the relation of Δn.
Encoding ADPCM data is as shown in Table 5.1.

Table 5-1: ADPCM data and quantization width change rate(f)

L4		L3	L2	L1	f	Condition (In=|dn|/Δn)
Dn>=0	Dn<0					
0	1	0	0	0	57/64	In <1/4
		0	0	1	57/64	1/4<= In <1/2
		0	1	0	57/64	1/2<= In <3/4
		0	1	1	57/64	3/4<= In <1
		1	0	0	77/64	1<= In <5/4
		1	0	1	102/64	5/4<= In <3/2
		1	1	0	128/64	3/2<= In <7/4
		1	1	1	153/64	7/4<= In

Conversion from the voice data to ADPCM data ends because of the above-mentioned operation.

⑤ Update of forecast value and width of quantization

When ADPCM data is obtained, the forecast value of the next step; ^xn+1
Width of quantization; Δn+1 is renewed.

$\hat{x}_{n+1} = (1-2*L4) * (L3+L2/2+L1/4+1/8) * \Delta n + \hat{x}_n$

$\Delta n+1 = f(L3, L2, L1) * \Delta n$: Δnmin=127, Δnmax=24576

*Initialization: Forecast value ^x1=0
Width of quantization Δ1=127

Hereafter, the voice analysis is done repeating the operation of ①-⑤ every each sampling time.

B. Procedure of ADPCM voice synthesis

It becomes an expression that the expression of the update of the forecast value and the width of the quantization indicated in item ⑤ of the analysis calculates the blended data. In a word, the forecast value becomes a synthetic sound and it will obtain it.

5-2: Register function
ADPCM sound source part is controlled by 17 registers of $00-$10.
(When bus control signal A1 is “1”, the register is accessed.)

It explains the function of each register as follows. An external memory in the sentence indicates RAM or ROM that OPNA manages.

□ Control register 1: $00
It is a register for the control of the start and the external memory access of ADPCM voice analysis/synthesis.

	D7	D6	D5	D4	D3	D2	D1	D0
$00	START	REC	MEM DATA	REPEAT	SP OFF	/	/	RESET

D0: It is a reset function at ADPCM voice synthesis. The voice synthesis is stopped when making it to “1” while executing it and it returns to the initial state. Please make REPEAT(D4) “0” when you reset it.
D3: The terminal SPOFF becomes “1” at “1”, and it uses it as a control signal for speaker OFF when ADPCM analysis and AD are converted.
D4: The repetition is set. It becomes repetition on at “1”, the same address section of an external memory is accessed repeatedly, and ADPCM voice synthesis is done.
D5: The memory that accesses ADPCM analysis/blended data is selected. It makes it to “0” at the memory of “1” and CPU management when an external memory is accessed.
D6: When the analysis data is written from ADPCM voice analysis and CPU in an external memory, it makes it to “1”.
D7: ADPCM voice analysis/start of synthesis, it is setting bit. The analysis and the synthesis start at time from which “1” stood in this bit when an external memory is accessed. Therefore, it is necessary to set all conditions necessary for analysis/synthesis before it starts. It starts at time when the ADPCM-DATA register of $08 was done in READ/WRITE when the memory of CPU management is accessed.

* RESET and REPEAT are functions that work only when an external memory is accessed.
* When START bit is made “0”, START bit is previously made “0”, and, next, the data of the remainder is reset.

□ Control register 2: $01
An external memory is specified, and it is specified to control and to output the DA/AD conversion ADPCM.

	D7	D6	D5	D4	D3	D2	D1	D0
$01	L	R	/	/	SAMPLE	DA/AD	RAM TYPE	ROM

D0: Specification of external memory. ROM at “1”, DRAM at “0”.
D1: Bit specification of DRAM.
It accesses it with *8bit at “1”, and *1bit at “0”.
D2: Specification of DA/AD conversion.
At “1”, the data written in the DAC DATA register of $0E is output specifying the DA conversion.
At “0”, the AD conversion is specified, 8bitPCM(two's complement) AD is converted into data.
D3: The DA/AD conversion starts at the time made “1”.
D6: At “1”, it outputs it to Lch.
D7: At “1”, it outputs it to Rch.

<<Start of DA/AD conversion>>
DA conversion It starts at time when setting SAMPLE(D3) and DA/AD(D2) of the DA output were made “1” in control register 2($01).
AD conversion It starts at time when SAMPLE(D3) was made “1”, after it is assumed “0” in DA/AD(D2), and “1” in SPOFF(D3) in control register 1($00).

□ Start address L/H:$02/$03
□ Stop address L/H:$04/$05
The start address and the stop address of DRAM and ROM are set.

	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
$03,$02	Start Address(H)								Start Address(L)							
$05,$04	Stop Address(H)								Stop Address(L)							

<<Address setting of start/stop>>

BANK			CAS ADDRESS								RAS ADDRESS								
2^2	2^1	2^0	A8	A7	A6	A5	A4	A3	A2	A1	A0	A8	A7	A6	A5	A4	A3	A2	A1	A0
START ADDRESS(H)								START ADDRESS(L)								0	0	0	0	0
STOP ADDRESS(H)								STOP ADDRESS(L)								1	1	1	1	1

*For DRAM(256k*1bit)
- BANK means the chip selection of eight DRAM.
- The data access is done by the unit of bit, and minimum resolution of addressing becomes the unit of 32bit(4byte).

*At ROM and the DRAM*8bit access
- BANK data (D7-D5) is set to the same value as the start address and the stop address.
- The data access is done by the unit of byte, and minimum resolution of addressing becomes 32 bytes.

□ Prescale L/H: $06,$07
The sampling frequency when AD including ADPCM analysis is converted, and DA is converted is specified. The range of specification is 2kHz-16kHz.

	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
$07,$06	PRESCALE(H)								PRESCALE(L)							
	/	/	/	/	/	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

fsample = ϕM / 2NPRE; NPRE=250-2047 (At ϕM = 8MHz)

(example) NPRE=500 at fsample=8kHz

□ ADPCM data: $08
When CPU accesses an external memory, it is a buffer register that the read write that stores ADPCM data is possible in ADPCM analysis/synthesis to the memory that CPU manages.

	D7	D6	D5	D4	D3	D2	D1	D0
$08	ADPCM DATA							

<<Composition of ADPCM data>>

D7	D6	D5	D4	D3	D2	D1	D0
Data n				Data n+1			
L4	L3	L2	L1	L4	L3	L2	L1

Because ADPCM data is data of 4bit, it becomes two data a byte. If high rank 4bit is nth data, subordinate position 4bit becomes the data of the n+l turn eyes following it.

□ DELTA-N L/H: $09, $0A

The sampling frequency at ADPCM voice synthesis is set. The interpolation coefficient to linear interpolate between each sampling by 55.5kHz is given at the same time.

	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
$0A,$09	DELTA-N(H)								DELTA-N(L)							
	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0

DELTA-N = (fsample/55.5kHz) * 2^{16} ;DELTA-N = 2362-2^{16}

(example) DELTA-N=9447 at fsample=8kHz

□ Level control: $0B
The output level of ADPCM voice synthesis is controlled from no sound (00) to maximum volume (FF) to 256 steps. This data is effective only to ADPCM voice synthesis output.

	D7	D6	D5	D4	D3	D2	D1	D0
$0B	LEVEL CONTROL							

□ Limit address L/H:$0C,$0D

It is a register that sets the limit value of the memory. It returns to 0 when getting to this address when the memory is accessed. A set value of this register is equal to the stop address or assumed to be a large value. At ADPCM speech analysis/synthesis, please set memory read/write.

	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
$0D,$0C	LIMIT ADDRESS(H)								LIMIT ADDRESS(L)							

□ DAC data: $0E

When DA is converted, the DA conversion is done by writing data in this register. The data format at the time of writing is two's complement 8bitPCM data.

	D7	D6	D5	D4	D3	D2	D1	D0
$0E	DAC DATA							

□ PCM data: $0F

It is a register only for reading to store the data that has been converted when AD is converted. Therefore, this register is done in READ and the PCM data is collected with CPU. The data format is two's complement 8bitPCM data.

	D7	D6	D5	D4	D3	D2	D1	D0
$0F	PCM DATA							

□ FLAG control: $10
Each flag of status 1 (or 0) is controlled. After the system is reset, D4, D3, and D2 are intitialized to “1”, others are “0”.

	D7	D6	D5	D4	D3	D2	D1	D0
$10	IRQ RESET	/	/	MASK ZERO	MASK BRDY	MASK EOS	MASK TIMERB	MASK TIMERA

D0: At “1”, regardless of timer A movement, the flag of timer A is masking done and it is assumed “0”.
D1: The mask does the flag of timer B as well as MASK TA.
D2: The mask does the EOS flag at “1”. At this time, when the end of ADPCM voice analysis and the synthesis, ends of read/write of an external memory, and the AD conversions are ended, the EOS flag is not generated.
D3: At “1”, the mask does the BRDY flag. At this time, data writing demand and reading demand (BRDY) the flags when it ADPCM voice analyzes, it synthesizes, and an external memory is accessed are not generated.
D4: At “1”, the mask does the ZERO flag.
D7: When writing it as “1”, mask bit of D4-D0 is disregarded (Rewriting bit is prohibited). All status flags are made “0” at the same time.

5-3: Status register
Status information is obtained by leading STATUS0 and 1. The event flag is composed of the flag only for timer flag, BUSY flag, and ADPCM. “1” stands from these flags when each event is generated. Moreover, the mask of a needless flag is also possible by flag control ($10).

Interrupt can be processed from the terminal !IRQ to CPU according to status information. When “1” stands in either of flag, the terminal !IRQ becomes LOW level, and generates the interrupt signal for CPU. (Because the terminal !IRQ is an open drain output, the terminal !IRQ and Wired of other devices can be connected.)

- STATUS0: $XX (When bus control A1 and A0 are “0”, it reads)
  There is no alterations necessary when the software developed with OPN is used because this register is the same composition as the status register of YM2203(OPN).

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	/	/	/	/	/	FLAG B	FLAG A

  D0: When the time set in timer A passes, it becomes “1”.
  D1: When the time set in timer B passes, it becomes “1”.
  D7: It becomes “1” while loading data into the register. This flag is effective only to the register of the FM sound source part. There is no wait time needed when the address write and the data write are done while seeing the flag.

- STATUS1: $XX (When bus control A1 is “1”, and A0 is “0”, it reads)
  It is a register that adds the status flag needed when ADPCM is analyzed to STATUS0. Therefore, FLAG A, FLAG B, and BUSY are the same to STATUS0 functions.

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	/	PCM BUSY	ZERO	BRDY	EOS	FLAG B	FLAG A

  D2: When ending ADPCM voice analysis/synthesis passes at one sampling cycle when AD/DA is converted, it becomes “1”.
  D3: When it ADPCM voice analyzes (synthesis), and the analysis of two data (4bit*2) (synthesis) ends, it becomes “1”. When the external memory write (read) and the write (read) ends by one data, it becomes “1”.
  D4: When the state of a no sound continues to 290msec or more while analyzing ADPCM voice, it becomes “1”.
  D5: It becomes “1” while executing ADPCM voice/synthesis.

RAM-WRITE (CPU->OPNA->RAM)

ADDR.	DATA	R/W	Comment
			◎Initialization
$10	$13	W	Flag BRDY and EOS are enabled.
$10	$80	W	Each flag is reset.
$00	$60	W	It changes to the memory write mode.
$01	$00/$02	W	The memory type is specified.
$02	$XX	W	The start address is set. (L)
$03	$XX	W	(H)
$04	$△△	W	The stop address is set. (L)
$05	$△△	W	(H)
$0C	$□□	W	The limit address is set. (L)
$0D	$□□	W	(H)
			◎Memory write
$08	$xx	W	Writing of data.
$10	$1B	W	Flag BRDY is reset.
$10	$13	W	Only flag EOS and BRDY are enabled.
$--		R	One status read.
			Loop If it is flag EOS "1", it ends writing.
			If it is flag BRDY "1", it writes it next data.
$00	$00	W	◎End process.
$10	$80	W	

RAM/ROM-READ (external memory→OPNA→CPU)

ADDR.	DATA	R/W	Comment
			◎Initialization
$10	$13	W	Flag BRDY and EOS are enabled.
$10	$80	W	Each flag is reset.
$00	$20	W	It changes to the memory read mode.
$01	$00/$02	W	The memory type is specified.
$02	$XX	W	The start address is set. (L)
$03	$XX	W	(H)
$04	$△△	W	The stop address is set. (L)
$05	$△△	W	(H)
$0C	$□□	W	The limit address is set. (L)
$0D	$□□	W	(H)
			◎Memory read
$08		R	Reading of data. (dummy read of the first amount twice)
$10	$1B	W	Flag BRDY is reset.
$10	$13	W	Only flag EOS and BRDY are enabled.
$--		R	One status read.
			Loop If it is flag BRDY "1", it reads it the next data.
			『Because the flag doesn't stand, the last two data is a thing read regardless of the flag.』
			If flag EOS is "1", it ends reading.
$00	$00	W	◎End process.
$10	$80	W	

Speech analysis (OPNA→external memory)

ADDR.	DATA	R/W	Comment
			◎Initialization
$10	$1B	W	Flag BRDY and EOS are enabled.
$10	$80	W	Each flag is reset.
$00	$68	W	It changes to speech analysis (memory) mode. SP OFF.
$01	$00/$02	W	The memory type is specified.
$02	$XX	W	The start address is set. (L)
$03	$XX	W	(H)
$04	$△△	W	The stop address is set. (L)
$05	$△△	W	(H)
$0C	$□□	W	The limit address is set. (L)
$0D	$□□	W	(H)
$06	$F4	W	Sampling rate setting. (L)
$07	$01	W	<8kHz: Npre=500> (H)
			◎Analysis start
$00	$E8	W	It the analysis begins by synchronizing with becoming of $00 and D7 “1”.
		R	Status 1 read.
			It stands by until “1” stands in flag EOS, and the analysis end is directed.
$00	$00	W	◎End process.
$10	$80	W	

Voice synthesis(external memory→OPNA)

ADDR.	DATA	R/W	Comment
			◎Initialization
$10	$1B	W	Flag EOS is enabled.
$10	$80	W	Each flag is reset.
$00	$20/$30	W	It changes to (memory) mode of the voice synthesis.
$01	$40-$42	W	The memory type is specified. It outputs it to Rch.
$02	$XX	W	The start address is set. (L)
$03	$XX	W	(H)
$04	$△△	W	The stop address is set. (L)
$05	$△△	W	(H)
$0C	$□□	W	The limit address is set. (L)
$0D	$□□	W	(H)
$09	$DE	W	Sampling rate setting. (L)
$0A	$24	W	<8kHz: △N=9438> (H)
$0B	$00-$FF	W	Setting of output level.
			◎Synthetic start
$00	$A0/$B0	W	It the synthesis begins by synchronizing with becoming of $00 and D7 “1”.
		R	Status 1 read.
			It stands by until “1” stands in flag EOS, and a synthetic end is directed.
	$A1	W	The synthesis is compulsorily discontinued.
$00	$00	W	◎End process.
$10	$80	W	

Speech analysis(OPNA→CPU)

ADDR.	DATA	R/W	Comment
			◎Initialization
$10	$17	W	Flag BRDY is enabled.
$10	$80	W	Each flag is reset.
$00	$C8	W	It changes to speech analysis (CPU) mode. SP OFF.
$06	$F4	W	Sampling rate setting. (L)
$07	$01	W	<8kHz: Npre=500> (H)
			◎Analysis start
$08		R	Data reading (the first dummy read)
$10	$80	W	Each flag is reset.
		R	One status read.
			If it is flag BRDY “1”, it reads it the next data.
$00	$48	W	◎End process.
$00	$00	W	
$10	$80	W	

Voice synthesis(CPU→OPNA)

ADDR.	DATA	R/W	Comment
			◎Initialization
$10	$17	W	Flag BRDY is enabled.
$10	$80	W	Each flag is reset.
$00	$80	W	It changes to speech analysis (CPU) mode.
$01	$C0	W	It outputs it to L and R.
$09	$DE	W	Sampling rate setting. (L)
$0A	$24	W	<8kHz: △N=9438> (H)
$0B	$xx	W	Volume setting.
			◎Analysis start
$08	$xx	W	Data writing
$10	$80	W	Each flag is reset.
		R	One status read.
			If it is flag BRDY “1”, it writes it the next data.
$00	$00	W	◎End process.
$10	$80	W	

AD conversion

ADDR.	DATA	R/W	Comment
			◎Initialization
$10	$1B	W	Flag EOS is enabled.
$10	$80	W	Each flag is reset.
$06	$F4	W	Sampling rate setting. (L)
$07	$01	W	<8kHz: Npre=500> (H)
$00	$08	W	Speaker OFF.
			◎Conversion process
$01	$08	W	AD beginning.
		R	One status read.
			If it is flag EOS “1”, it reads the PCM data.
$0F	$xx	R	PCM data read.
$10	$80	W	The flag is reset.
$00	$00	W	◎End process.
$10	$80	W	

DA conversion

ADDR.	DATA	R/W	Comment
			◎Initialization
$10	$1B	W	Flag EOS is enabled.
$10	$80	W	Each flag is reset.
$06	$F4	W	Sampling rate setting. (L)
$07	$01	W	<8kHz: Npre=500> (H)
			◎Conversion process
$01	$CC	W	DA beginning
$0E	$xx	W	DAC data writing
		R	One status read.
			If it is flag EOS “1”, it resets and writing of the next data.
$10	$80	W	The flag is reset.
$00	$00	W	◎End process.
$10	$80	W	